REMARKS

Acceptance of this Submission pursuant to USPTO RCE practice as well as withdrawal of the finality of the last Office Action is respectfully requested. Moreover, reconsideration and allowance of the above-identified application, as currently amended, is also respectfully requested.

By the present Amendment, independent claim 15 has been amended so as to further clarify the invention including to highlight various patentable aspects thereof. Supportive discussion regarding the current claim amendments is based, for example, on the description from page 13, line 10, to page 15, line 13, of the Specification and Figs. 18 and 19 of the drawings which to relate the operation of the disclosed example second embodiment, although not limited thereto.

A key aspect of the invention is that an interval of inputted information (i.e., an instruction or data) to a functional circuit block is used as an input of the prediction circuit that predicts the power status. Using the Fig. 2 embodiment as an example, prediction circuit P1 is used to control a power status circuit D1 which, in turn, controls the power level of a functional circuit K1. As is shown in the embodiments of Figs 1 and 2 et seq., both the prediction circuit P (P1) and the functional circuit K (K1) receive the same input signal which can be either an instruction or data. Because the prediction circuit receives the same instruction or data which is inputted into the functional circuit block, no additional instructions or data are necessary from other computation devices for the prediction circuit to control the power status control circuit which controls the power status of the functional circuit. Said differently, the prediction circuit is able to operate independently without the aid of other

computation devices. For example, if there is no incoming information at input I for a predetermined time, the power status control circuit (e.g., D in Fig. 1, D1 in Fig. 2, etc.) shifts the power status of the functional circuit block (e.g., K or K1) to a low-power status. This power shifting operation is achieved independently of any desired computation device. (Page 10, line 9, to page 11, line 3, of the original Specification.)

As is shown by the discussion of Figs. 18 and 19 of the drawings, such as it relates to the example Fig. 2 embodiment, if after an interval of time, e.g., after a number of clock pulses are counted, there is no effective information received on the input I, the power status control circuit D1 shifts the power status of the functional block KB to low-power status. Once operation is changed to that of a high-power status when information (instruction or data) is received at input I, the high-power status for the functional circuit block remains in effect for a set number of clock pulses. If new information (instruction or data) is received within a set interval, which may be defined as a set number of clock pulses, the power status of the functional circuit block will remain at a high-power status. However, if information (data or instruction) is not received within that interval, e.g., as determined by the clock pulse count, the power status of the functional circuit block is reverted to that of a low-power status. Such control of the power status control circuit by the prediction circuit, independently of other computation devices, which takes into account "an interval between successive instructions or data which are inputted to both the functional circuit block and the prediction circuit " is now particularly highlighted in independent claim 15 and, therefore, also with regard to the corresponding

dependent claims thereof. It is submitted, a scheme as that now set forth in base claim 15 and further, according to the corresponding dependent claims thereof is a clear patentable improvement over that previously known including over the teachings of the art documents, as applied in the previously standing rejections.

Reconsideration as well as withdrawal of the rejections covering claims 15 – 18 and 20 – 28 based on Datar [et al.], applied in the rejection of claims 15 – 17 under 35 U.S.C. 102(e), and also applied as the primary reference in combination with various ones of the secondary references to Dean, et al., Ranta-aho, et al., Kataoka, et al., Brouwer, Mohamed, et al. and Takayama, et al., applied to different ones of the dependent claims, is respectfully requested. As discussed above, base claim 15 has been further amended to highlight that the controlling performed by the prediction circuit, which is effected independently of other computation devices, is also based on the interval between successively inputted information (instructions or data) to both the functional circuit block and the prediction circuit. It is submitted, Datar neither disclosed nor suggested such featured aspects as that set forth according to claims 15+. In fact, even if one of ordinary skill would have applied the teachings of Datar in combination with other ones of the cited secondary references, such as in the manner as that applied in the respective rejections, the invention according to claims 15+ still could not have been realizable.

It is submitted, neither Datar, nor any of the other cited references, applied individually or in any combination, disclosed or suggested the scheme called for in independent claim 15 and further according to the corresponding dependent claims thereof, in which the interval between successive information (instructions or data)

which are inputted to both the functional circuit block and the prediction circuit is used by the prediction circuit to predict the power status of the functional circuit block, this being done, also, independently of other computation circuits.

Datar, requires a compiler that is separate from either the power control code state machines of Fig. 3 or the central power control block of Fig. 4, in order to implement its control operations. With regard to Fig. 3 of Datar, control is carried out for functional circuits using power control code state machines (e.g., 301a and 301b) in the respective processors (e.g., 201a and 201b). With regard to Fig. 4 thereof, Datar replaces the power control code state machines with a central power control block (e.g., 401). (Column 1, lines 7 et seq. of Datar.)

According to Datar's teachings, a dynamic power control code must first be generated by use of a compiler and, also, the state machine 301 (301a and 301b) effects control of the turn-on/turn-off of the circuit blocks 202 – 206 based on the generated power control code. Discussion related thereto is detailed from column 5, line 55, to column 6, line 45, in Datar. Accordingly, the designer of the software, firmware and compiler must be aware of the characteristic details thereof including their behavior and respond accordingly. That is, the power control code related to Datar's teachings, it is submitted, does not operate independently of other computation devices, as is required according to that set forth in base claim 15. Datar, et al.'s teachings appear to correspond to earlier known (conventional) efforts at least in the point that the design engineer must necessarily recognize the entire behavior of the system, in clear contradistinction with that according to the invention defined by independent claim 15 and, further, according to corresponding dependent

claims thereof. It is submitted, Datar's scheme cannot control the behavior of an individual circuit block that is not described within the system by the compiler. Because the design engineer who purchases IP or receives IP licenses for implementing the semiconductor device, typically, cannot access the internal mechanisms of the protected IP (intellectual property) purchases, controlling of the power being applied thereto, according to the present invention, is autonomously decentralized, which is an important aspect thereof. Such, it is submitted, clearly, was not taught by Datar.

According to the invention defined in claims 15+, since it predicts a power status by use of, also, the interval of applied information (i.e., instruction or data), in which the input may be commonly applied to both the prediction circuit or any number of circuit blocks, the behavior of the specific circuit components/elements of such circuit blocks can be effectively controlled. It is submitted, such does not appear to be the case with Datar, Datar applied separately or in combination with any of the other secondary references.

In view of the above-noted shortcomings of the primary reference to Datar, insofar as teaching or suggesting the featured aspects of the prediction circuit as that now set forth in independent claim 15 and further according to the corresponding dependent claims thereof, the invention, it is submitted, could not have been anticipated nor rendered obvious therefrom. Moreover, none of the applied secondary references, including the references to Dean, et al., Ranta-aho, et al., Kataoka, et al., Brouwer, Mohamed, et al. and Takayama, et al. (JP patent publication), relied on in the final Office Action rejections, overcome the

shortcomings of Datar. Therefore, allowance of independent claim 15, as now amended, as well as of the corresponding dependent claims thereof, is respectfully requested.

Incidentally, objected claim 19, which was previously indicated as otherwise allowable (see Item 42 of the Detailed Action to the Final Office Action), has be re-presented in a self-contained format as newly added independent claims 29, combining the contents of previously pending base claim 15, intervening claim 18 and dependent claim 19.

Therefore, in view of the amendments presented above together with these accompanying remarks, withdrawal of the outstanding rejections as well as favorable action on the currently pending claims and an earlier formal notification of allowance of the above-identified application is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 520.40524X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,
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